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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,152	02/06/2002	Sang-Eun Lee	8750-17	7500

7590 09/25/2003

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,152	LEE ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *09 July 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings were received on July 9, 2003. These drawings are approved.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 7, and 10-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Simmons (6265232).

Regarding claim 7, Simmons discloses [see Fig. 1] a wafer defect map (10), comprising: a schematic representation of a semiconductor wafer (12), including demarcations (scribe lines 18) corresponding to the location of chip (die 16) boundaries; and a plurality of markings [not shown in the figure], each marking corresponding to a wafer defect (14), wherein locations of the markings on the wafer map (10) correspond to locations of the defects (14) on the wafer (12), and wherein each marking is configured to identify a type of defect (14).

Regarding claim 10, Simmons discloses the location and type of wafer defects (14) is determined using a semiconductor defect inspection instrument (not shown) [see column 3 lines 44-45].

Regarding claim 11, Simmons discloses [see Fig. 1] a method of statistically analyzing defects on a semiconductor wafer (12), said method comprising: identifying a location and type

of wafer defects (14) [see column 3 lines 43-62]; determining a composition of the wafer defects (14) [see column 4, lines 3-65 and Figs. 3-4; preparing a wafer defect map (10) to visually represent the location and type of the wafer defects (14) [see Fig. 1]; and preparing one or more charts [see Figs. 3-4] to statistically represent defect (14) characteristics.

Regarding claim 12, Simmons discloses markings are placed on the wafer defect map (10) corresponding to defect locations (14).

Regarding claim 14, Simmons discloses identifying a location and type of wafer defects (14) comprises using an optical or scanning electron microscope (not shown) to identify the location and type of wafer defects (14) [see column 3 lines 44-54].

Regarding claim 15, Simmons disclose a determining a composition of the wafer defects (14) comprises performing an AES analysis [not shown] on the defects (14) to determine the compositions thereof [see col. 3 lines 44-62].

Regarding claim 16, Simmons discloses preparing one or more charts [see Figs. 3-4] comprises constructing a table comprising columns corresponding to defect type [bottom of Fig. 4], defect composition [Fig. 3], defect cause [bottom of Fig. 4], and defect location [see Fig. 3].

Regarding claim 17, Simmons discloses preparing one or more charts [see Figs. 3-4] comprises preparing a bar graphs representing the number of defects 914) according to defect type.

Regarding claim 18, Simmons discloses preparing a wafer defect map (10) to visually represent the location and type of the wafer defects (14), and preparing one or more charts [see Figs. 3-4] to statistically represent defect characteristics are performed electronically [see col. 3, lines 63- col. 4, line 34].

Regarding claim 19, Simmons discloses identifying a location and type of wafer defects (14), and determining a composition of the wafer defects (14) are also performed electronically [see col. 3, lines 63- col. 4, line 34].

Regarding claim 20, Simmons discloses analyzing the one or more charts [see Figs. 3-4] to determine appropriate corrective action in a wafer fabrication process [see column 6 lines 21-36].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-6, 8-9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmons (6265232).

Regarding claim 1, Simmons discloses a method of classifying defect chips (die 16) [see Fig. 2], said method comprising: finding defect locations (14) on a wafer (12) using a

semiconductor defect inspection instrument (not shown) [see column 3 lines 51-57]; analyzing the defect composition using the semiconductor defect inspection instrument [see column 3 lines 43-62]; and marking defect locations (14) on a wafer map (10). However, he does not disclose using the different types of marks to identify different types of defect. It is well known to use different type marks where needed. (see MPEP 2144.04 *In re Seid*, 161 F.2d 229, 73 USPQ 431 (CCPA 1947)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use different types of marking on the wafer map since the different types of marking, which relates to ornamentation that has no mechanical function, would provide support in a selective manner to each individual user that marks the wafer to classify defect chips.

Regarding claims 2-3, Simmons discloses marking defect locations (14) on a wafer map (10). However, he does not disclose using the different types of marks according to shape. It is well known to use different type marks according to shape or color where needed. (see MPEP 2144.04 *In re Seid*, 161 F.2d 229, 73 USPQ 431 (CCPA 1947)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use different types of marking on the wafer map since the different types of marking, which relates to ornamentation that has no mechanical function, would provide support in a selective manner to each individual user that marks the wafer to classify defect chips.

Regarding claim 4, Simmons discloses graphing defect characteristics [see Figs. 3-4] concurrently with marking defect locations (14) on the wafer map (10).

Regarding claim 5, Simmons discloses storing [via bins 1-6] and analyzing defect characteristics electronically using software [see column 3 line 63- column 4, line 32].

Regarding claim 6, Simmons discloses using the marks (14) on the wafer map (10) to prepare graphs to assist in statistically analyzing the defects.

Regarding claims 8-9 and 13, Simmons discloses marking defect locations (14) on a wafer map (10). However, he does not disclose using the different types of marks according to shape. It is well known to use different type marks according to shape or color where needed. (see MPEP 2144.04 *In re Seid*, 161 F.2d 229, 73 USPQ 431 (CCPA 1947)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use different types of marking on the wafer map since the different types of marking, which relates to ornamentation that has no mechanical function, would provide support in a selective manner to each individual user that marks the wafer to classify defect chips.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tandy et al (6524881), Phan et al (6559457) disclose a method and apparatus for marking a semiconductor wafer or device.

8. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (703) 305-1653. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
September 9, 2003

EVAN PERT
PRIMARY EXAMINER